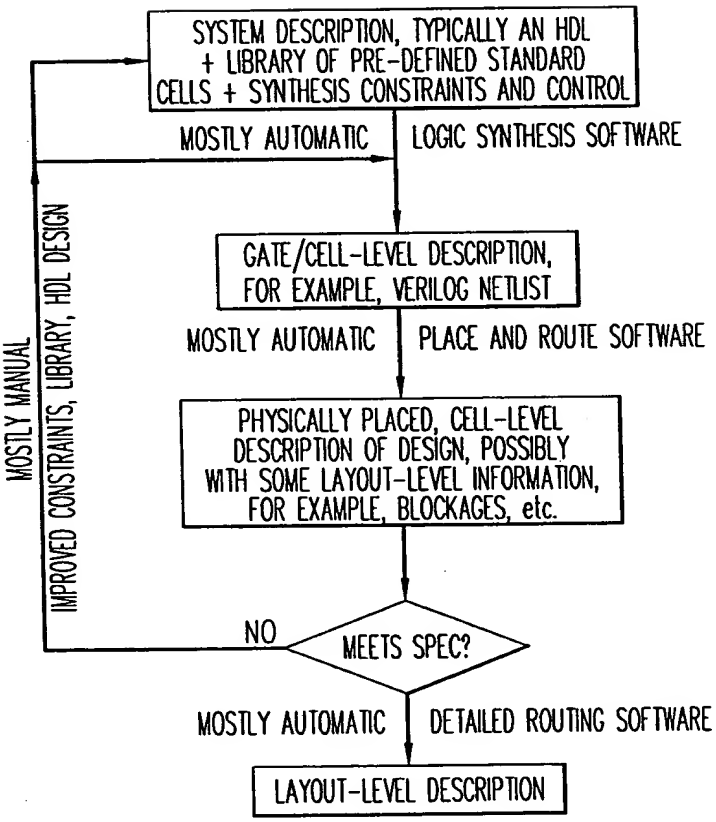

FIG. 1

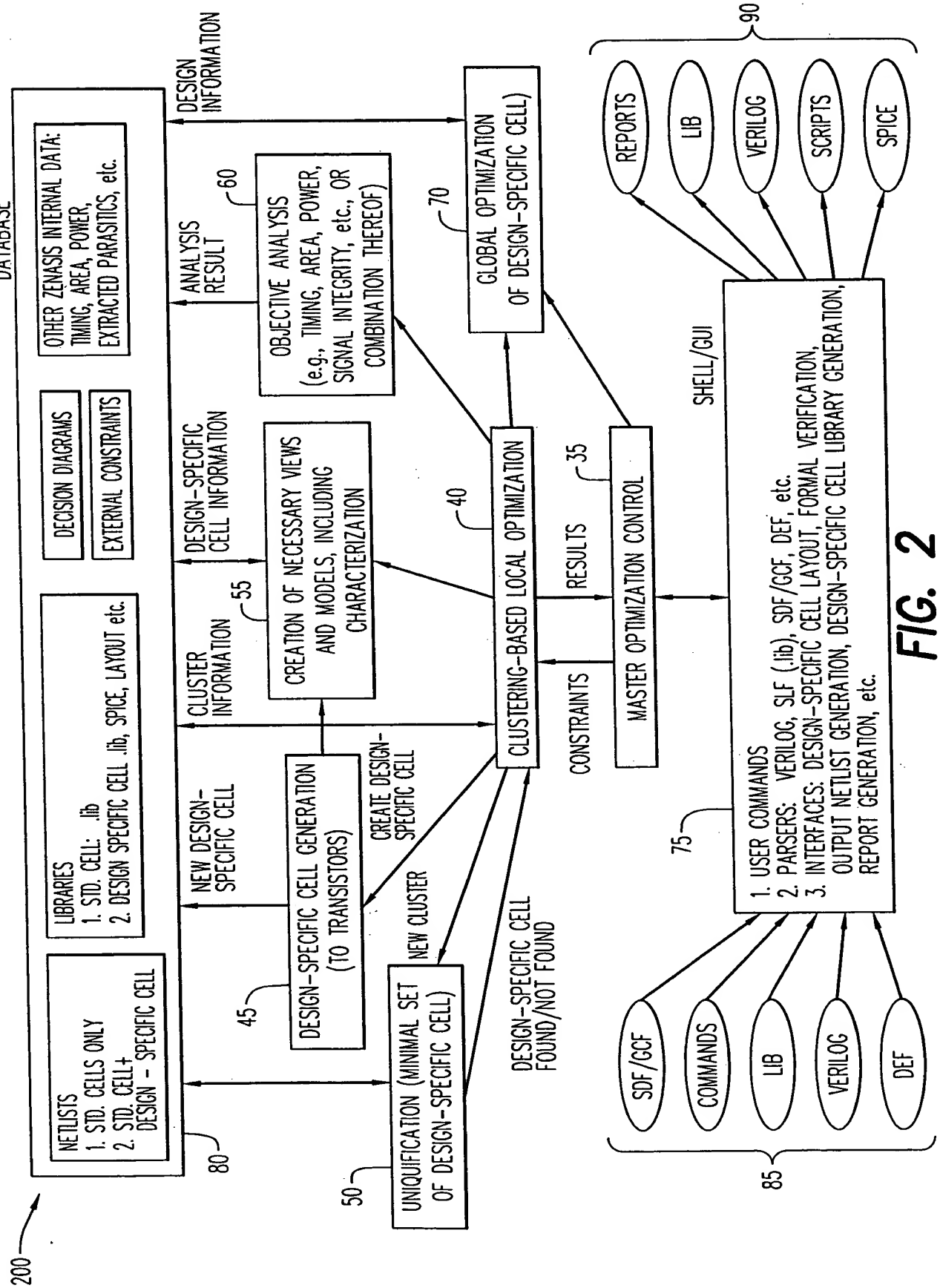
200
DATABASE
NETLISTS
1. STD. CELLS ONLY
2. STD. CELL+ DESIGN - SPECIFIC CELL
80
LIBRARIES
1. STD. CELL: .lib
2. DESIGN SPECIFIC CELL .lib, SPICE, LAYOUT etc.
DECISION DIAGRAMS
EXTERNAL CONSTRAINTS
OTHER ZENASIS INTERNAL DATA: TIMING, AREA, POWER, EXTRACTED PARASITICS, etc.
DESIGN INFORMATION
CLUSTER INFORMATION
NEW DESIGN-SPECIFIC CELL
DESIGN-SPECIFIC CELL INFORMATION
ANALYSIS RESULT
60
OBJECTIVE ANALYSIS (e.g., TIMING, AREA, POWER, SIGNAL INTEGRITY, etc., OR COMBINATION THEREOF)
55
CREATION OF NECESSARY VIEWS AND MODELS, INCLUDING CHARACTERIZATION
45
DESIGN-SPECIFIC CELL GENERATION (TO TRANSISTORS)
CREATE DESIGN-SPECIFIC CELL
50
UNIQUIFICATION (MINIMAL SET OF DESIGN-SPECIFIC CELL)
NEW CLUSTER
DESIGN-SPECIFIC CELL FOUND/NOT FOUND
40
CLUSTERING-BASED LOCAL OPTIMIZATION
70
GLOBAL OPTIMIZATION OF DESIGN-SPECIFIC CELL)
RESULTS
35
CONSTRAINTS
MASTER OPTIMIZATION CONTROL
SHELL/GUI
75
1. USER COMMANDS
2. PARSERS: VERILOG, SLF (.lib), SDF/GCF, DEF, etc.
3. INTERFACES: DESIGN-SPECIFIC CELL LAYOUT, FORMAL VERIFICATION, OUTPUT NETLIST GENERATION, DESIGN-SPECIFIC CELL LIBRARY GENERATION, REPORT GENERATION, etc.
90
REPORTS
LIB
VERILOG
SCRIPTS
SPICE
85
SDF/GCF
COMMANDS
LIB
VERILOG
DEF

FIG. 2

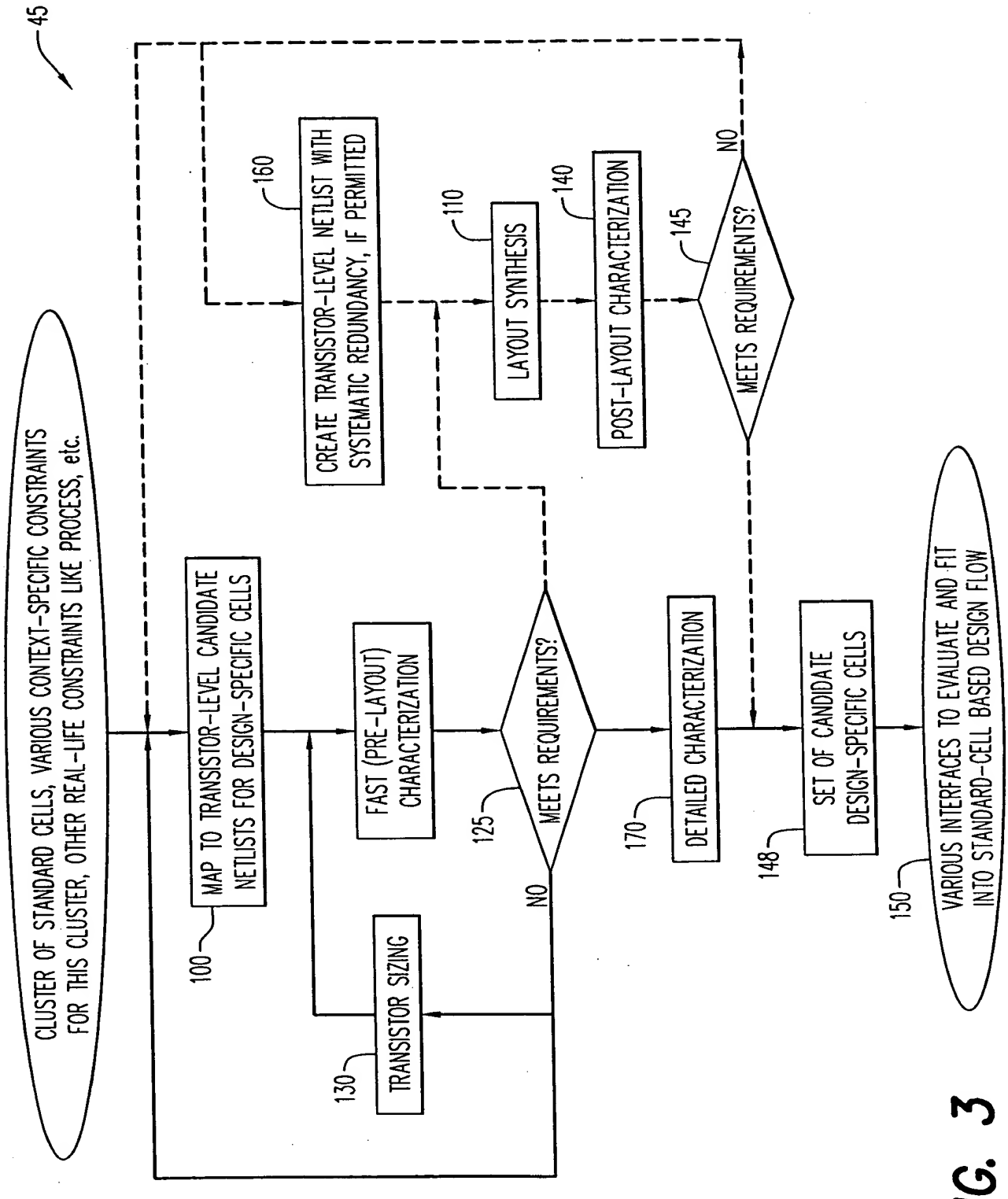
45
CLUSTER OF STANDARD CELLS, VARIOUS CONTEXT-SPECIFIC CONSTRAINTS FOR THIS CLUSTER, OTHER REAL-LIFE CONSTRAINTS LIKE PROCESS, etc.
100
MAP TO TRANSISTOR-LEVEL CANDIDATE NETLISTS FOR DESIGN-SPECIFIC CELLS
160
CREATE TRANSISTOR-LEVEL NETLIST WITH SYSTEMATIC REDUNDANCY, IF PERMITTED
110
LAYOUT SYNTHESIS
140
POST-LAYOUT CHARACTERIZATION
145
MEETS REQUIREMENTS?
NO
FAST (PRE-LAYOUT) CHARACTERIZATION
125
MEETS REQUIREMENTS?
NO
130
TRANSISTOR SIZING
170
DETAILED CHARACTERIZATION
148
SET OF CANDIDATE DESIGN-SPECIFIC CELLS
150
VARIOUS INTERFACES TO EVALUATE AND FIT INTO STANDARD-CELL BASED DESIGN FLOW

FIG. 3

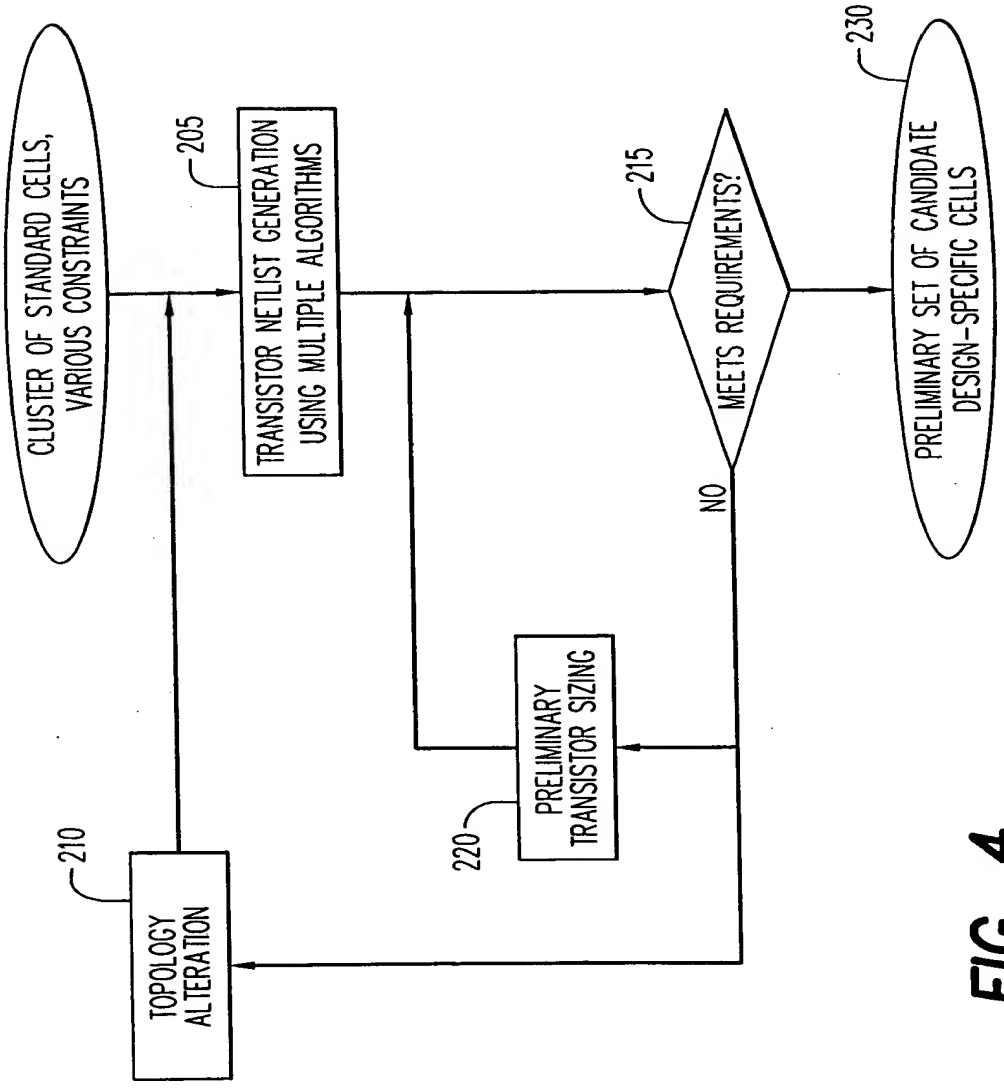
CLUSTER OF STANDARD CELLS, VARIOUS CONSTRAINTS
205
TRANSISTOR NETLIST GENERATION USING MULTIPLE ALGORITHMS
215
MEETS REQUIREMENTS?
NO
230
PRELIMINARY SET OF CANDIDATE DESIGN-SPECIFIC CELLS
220
PRELIMINARY TRANSISTOR SIZING
210
TOPOLOGY ALTERATION

FIG. 4

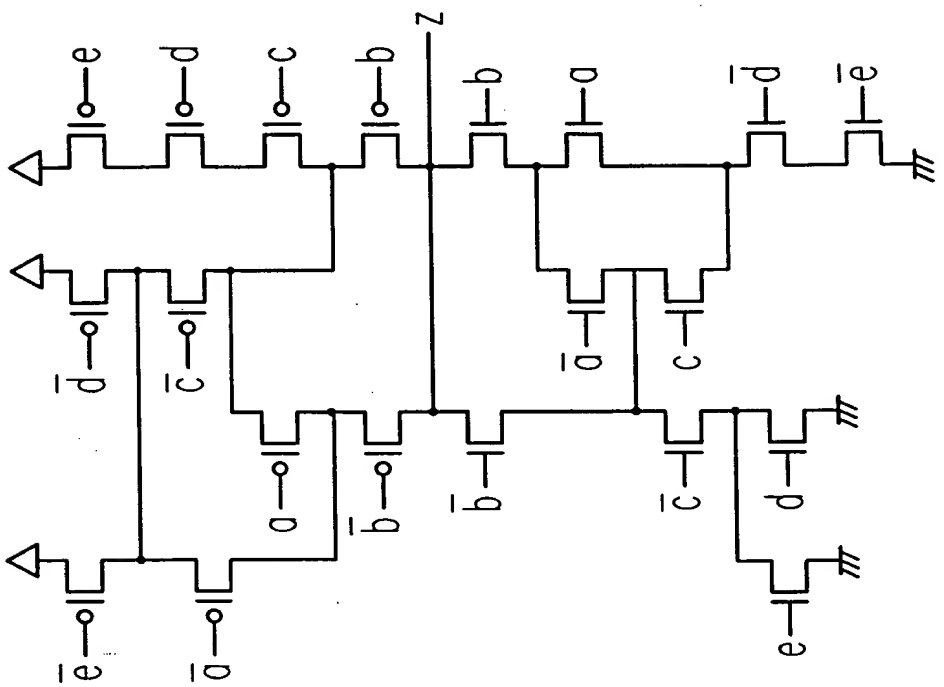

FIG. 5b

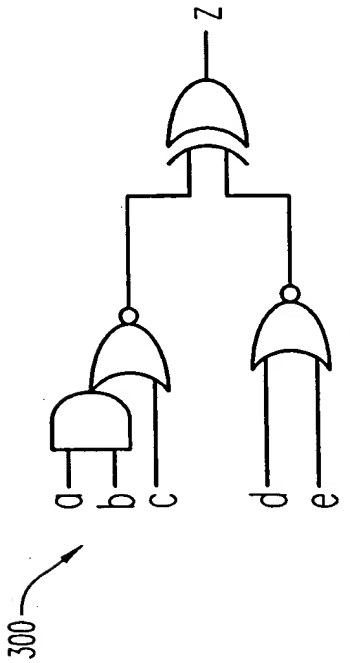

FIG. 5a

CRITICAL PATH TO z THROUGH b

⇧ DELAY FROM b TO z : 0.33 ns

⇧ DESIGN-SPECIFIC CELL DELAY : 0.14 ns

FIG. 5c

CRITERIA	ORIGINAL	OPTIMIZED
# OF CELLS	8	1
# OF TRANSISTORS	32	17
# OF WIRES (INCL. I/O)	12	5

FIG. 6c

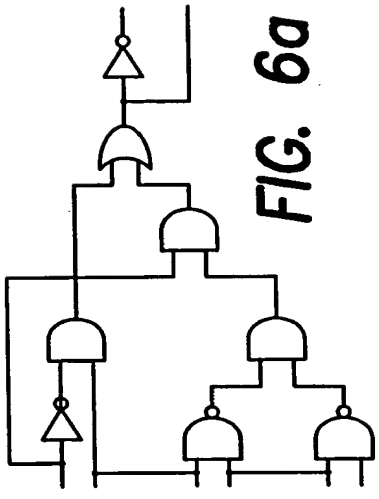

FIG. 6a

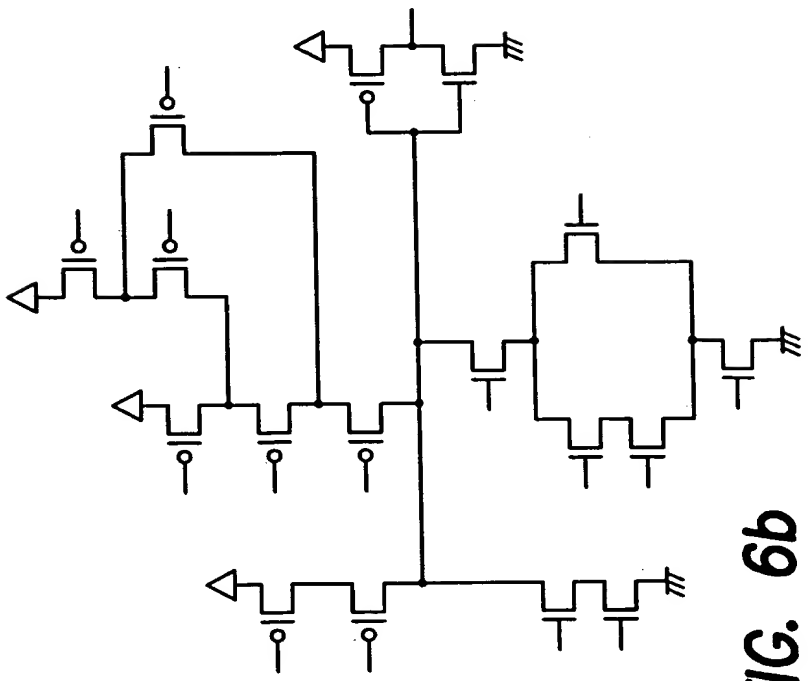

FIG. 6b

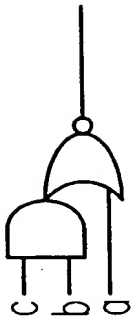

FIG. 7a

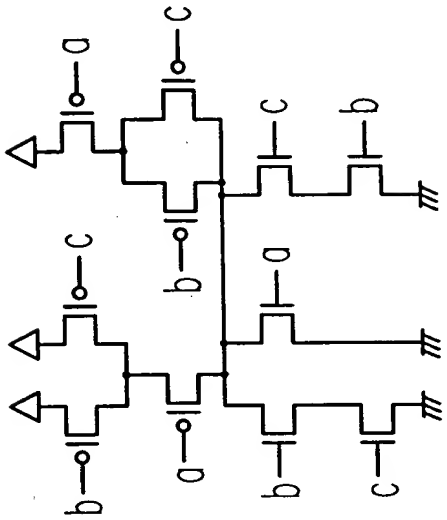

FIG. 7c

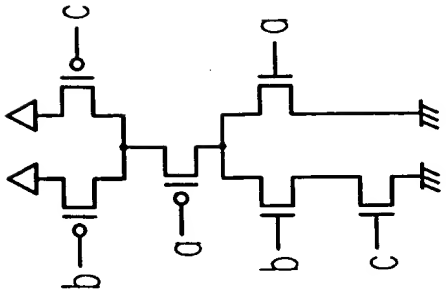

FIG. 7b